What is claimed is:

1. A method for forming an interconnect structure with dielectric barrier, comprising the steps of:

providing a semiconductor substrate with a first dielectric layer formed thereon, wherein a plurality of conductive lines are formed with a conductive plug thereon in the first dielectric layer;

removing the first dielectric layer to leave a plurality of stacked structures formed by the conductive line and the conductive plug thereon;

forming a conformal dielectric barrier on surfaces of the stacked structures; and

blanketly forming a second dielectric layer over the dielectric barrier to form an inter-metal dielectric (IMD) layer for insulating the stacked structures.

2. The method as claimed in claim 1, wherein the etching stop layer comprises oxygen-containing material.

3. The method as claimed in claim 2, wherein the oxygen-containing material is silicon oxycarbide (SiCO).

4. The method as claimed in claim 1, wherein the first dielectric layer comprises a plurality of oxygen-free dielectric layers.

5. The method as claimed in claim 4, wherein the oxygen-free material comprises pure silicon carbide, P-SiLK or other porous low-k dielectric.

6. The method as claimed in claim 1, wherein the conductive line comprises copper or copper aluminum alloy.

7. The method as claimed in claim 1, wherein the conductive plug comprises copper or copper aluminum alloy.

8. The method as claimed in claim 1, wherein the dielectric barrier comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN) with a dielectric constant of 4.5-5.0.

9. The method as claimed in claim 1, wherein the second dielectric layer comprises carbon-incorporated silicon oxide (SiOC) with a dielectric constant of 2.5-3.0.

10. A method for forming a interconnect structure with dielectric barrier, comprising the steps of:

providing a semiconductor substrate with an oxygen-containing etching stop layer and a oxygen-free first dielectric layer sequentially formed thereon, wherein a plurality of conductive lines are formed with a conductive plug thereon in the first dielectric layer;

removing the oxygen-containing first dielectric layer by etchant comprising N_2 and H_2 to leave a plurality of stacked structures formed by

the conductive lines and each conductive plug thereon;

depositing a conformal dielectric barrier on surfaces of the stacked structures; and

blanketly forming a second dielectric layer with at least one air gap over the dielectric barrier to form an inter-metal dielectric (IMD) layer for insulating the stacked structures.

11. The method as claimed in claim 10, wherein the oxygen-containing etching stop layer comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN) with a dielectric constant of 4.5-5.0.

12. The method as claimed in claim 10, wherein the oxygen-free first dielectric layer comprises a plurality of oxygen-free dielectric layers.

13. The method as claimed in claim 12, wherein the oxygen-free dielectric layers comprise pure silicon carbide, P-SiLK or other porous low-k dielectric.

14. The method as claimed in claim 10, wherein the conductive line comprises copper or copper aluminum alloy.

15. The method as claimed in claim 10, wherein the conductive plug comprises copper or copper aluminum alloy.

16. The method as claimed in claim 10, wherein the dielectric barrier comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN) with a dielectric constant of 4.5-5.0.

17. The method as claimed in claim 10, wherein the second dielectric layer comprises carbon-incorporating silicon oxide (SiOC) with a dielectric constant of 2.5-3.0.

18. An interconnect structure with dielectric barrier, comprising:

a semiconductor substrate;

a plurality of stacked structures formed thereon, wherein each stacked structure comprises a conductive line and a conductive plug thereon;

a conformal dielectric barrier over the surfaces of the stacked structures; and

a blanket second dielectric layer formed over the dielectric barrier to form an inter-metal layer for insulation thereof.

19. The interconnect structure as claimed in claim 18, further comprising an etching stop layer disposed between the semiconductor substrate and the dielectric barrier.

20. The interconnect structure as claimed in claim 18, wherein the etching stop layer comprises oxygen-containing material.

21. The interconnect structure as claimed in claim 20, wherein the oxygen-containing material comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN).

22. The interconnect structure as claimed in claim 18, wherein the first dielectric layer comprises a plurality of oxygen-free dielectric layers.

23. The interconnect structure as claimed in claim 22, wherein the oxygen-free dielectric layers comprise silicon carbide, P-SiLK or other porous low-k dielectric.

24. The interconnect structure as claimed in claim 18, wherein the conductive line comprises copper or copper aluminum alloy.

25. The interconnect structure as claimed in claim 18, wherein the conductive plug comprises copper or copper aluminum alloy.

26. The interconnect structure as claimed in claim 18, wherein the dielectric barrier comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN) with a dielectric constant of 4.5-5.0.

27. The interconnect structure as claimed in claim 18, wherein the second dielectric layer comprises carbon-

incorporated silicon oxide (SiOC) with a dielectric constant of 2.5-3.0.

28. The interconnect structure as claimed in claim 18, further comprising at least one air-gap in the second dielectric layer between the stacked structures.

29. An interconnect structure with dielectric barrier, comprising:

a semiconductor substrate;

a pair of stacked structures formed thereon, wherein each stacked structure comprises a conductive line and a conductive plug thereon; and

a conformal dielectric barrier disposed along sidewalls of each stacked structure.

30. The interconnect structure as claimed in claim 29, further comprising a blanket second dielectric layer formed on the dielectric barrier to form an inter-metal layer.

31. The interconnect structure as claimed in claim 29, wherein the dielectric barrier is disposed along the substrate between the stacked structures.

32. The interconnect structure as claimed in claim 29, further comprising an etching stop layer disposed between the semiconductor substrate and the dielectric barrier.

33. The interconnect structure as claimed in claim 32, wherein the etching stop layer comprises oxygen-containing material.

34. The interconnect structure as claimed in claim 33, wherein the oxygen-containing material comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN).

35. The interconnect structure as claimed in claim 29, wherein the first dielectric layer comprises a plurality of oxygen-free dielectric layers.

36. The interconnect structure as claimed in claim 35, wherein the oxygen-free dielectric layers comprise silicon carbide, P-SiLK or other porous low-k dielectric.

37. The interconnect structure as claimed in claim 29, wherein the conductive line comprises copper or copper aluminum alloy.

38. The interconnect structure as claimed in claim 29, wherein the conductive plug comprises copper or copper aluminum alloy.

39. The interconnect structure as claimed in claim 29, wherein the dielectric barrier comprises silicon oxycarbide (SiCO) or silicon carbonitride (SiCN) with a dielectric constant of 4.5-5.0.

40. The interconnect structure as claimed in claim 30, wherein the second dielectric layer comprises carbon-incorporated silicon oxide (SiOC) with a dielectric constant of 2.5-3.0.

41. The interconnect structure as claimed in claim 30, further comprising at least one airgap in the second dielectric layer between the stacked structures.